Module Introduction

PURPOSE:

- This module, ColdFire Application-specific Peripherals, provides an overview of the relationship between ColdFire and various application-specific peripherals. The intent is to provide a baseline of knowledge related to the ColdFire processor product line's integration.

OBJECTIVES:

- Identify the features and operation of the 10/100 Fast Ethernet Media Access Controller (MAC).
- Identify the features and operation of the Universal serial Bus (USB) device module.
- Identify the features and operation of the queued serial peripheral interface (QSPI) module.
- Identify the features and operation of the physical layer interface controller (PLIC).
- Identify the features and operation of the pulse width modulation (PWM) module.

CONTENT:

- 16 pages
- 3 questions

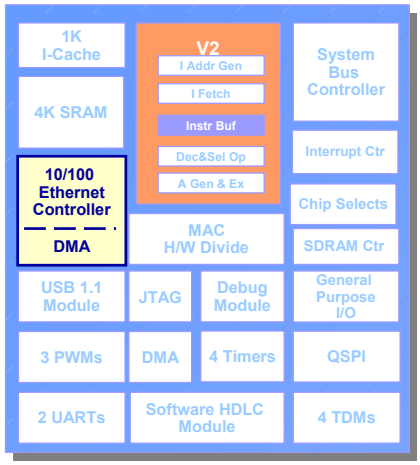
LEARNING TIME:

- 40 minutes

This module, ColdFire Application Specific Peripherals, provides an overview of the relationship between ColdFire and various application-specific peripherals. The intent is to provide a baseline of knowledge related to the ColdFire processor product line's integration.

In this module you will learn the features and operation of the 10/100 Fast Ethernet Media Access Controller (MAC). You will learn the attributes and functionality of the universal serial bus device module. Next, you will examine the features and operations of the queued serial peripheral interface module. Then, you will review the physical layer interface module's features and operations. Finally, you will learn the attributes and operations of the pulse width modulation module.

10/100-Mbit Fast Ethernet MAC



- **Fully IEEE 802.3 standard compliant**
- **Supported interfaces :**
  - **10 Mbps 7-wire**
  - **10/100 Mbps 18-wire MII**
- **Supported data rates :**
  - **10 Mbps full duplex and half duplex operation**
  - **100 Mbps half duplex operation**
  - **100 Mbps full duplex operation**
- **Dedicated DMA**
- **FIFOs :**
  - **Large on-chip transmit and receive FIFOs to support a variety of bus latencies**
- **Off-chip descriptor rings/buffers permit wide user capabilities and flexibility**

Let's begin examining the features of ColdFire's V2 by learning the new features of the Fast Ethernet Controller (FEC) module. The MCF5272's integrated Fast Ethernet Media Access Controller (MAC) performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. It requires an external interface adaptor and transceiver function to complete the interface to the media.

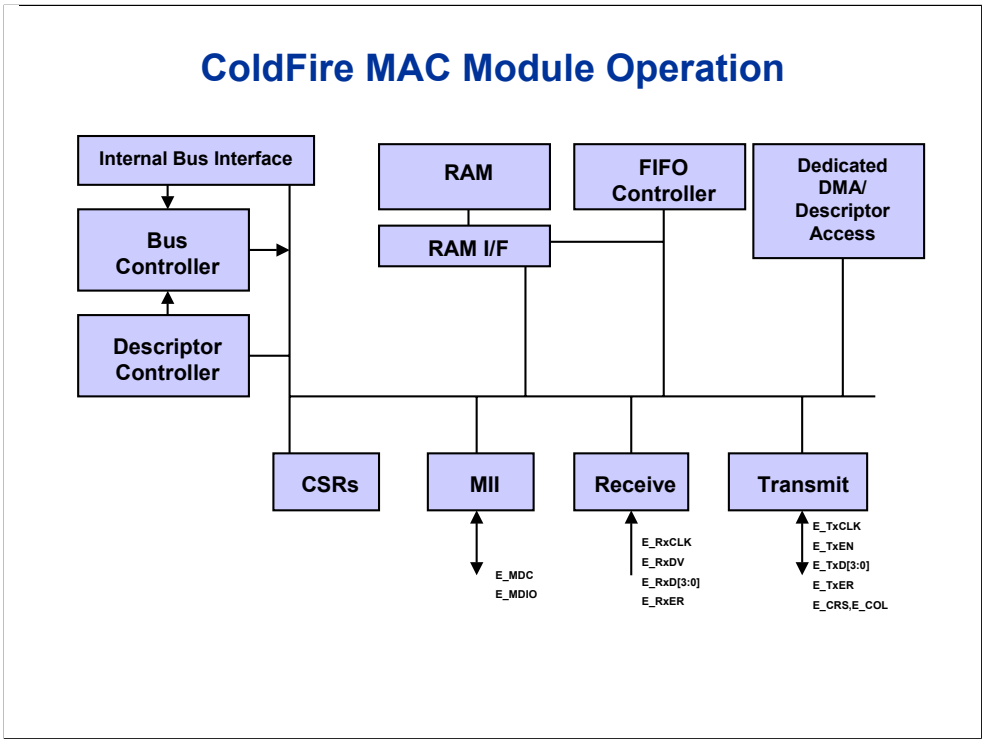
The FEC incorporates a number of new features. First, it is in full compliance with the IEEE 802.3 standard.

Second, it supports three different physical interfaces: 100 Mbps 802.3 media independent interface (MII), 10 Mbps 802.3 MII, and the 10 Mbps seven-wire interface.

Third, the half-duplex **and full-duplex** 100 Mbps operation **require a** system clock frequency **equal to or greater than** 50 MHz. It includes 448 bytes total on-chip transmit and receive First In First Out (FIFO) memory to support a range of bus latencies. Retransmission from the transmit FIFO following a collision does not use a processor bus. In addition, automatic internal flushing of the receive FIFO for runts and collisions is done without using a processor bus.

The off-chip descriptor rings/buffers of the FEC permits wide user capabilities and flexibility.

Finally, the FEC has a dedicated DMA.



Let's look at ColdFire's FEC module in more detail. The FEC is implemented using a combination of hardware and microcode. The figure here shows a functional block diagram of this module.

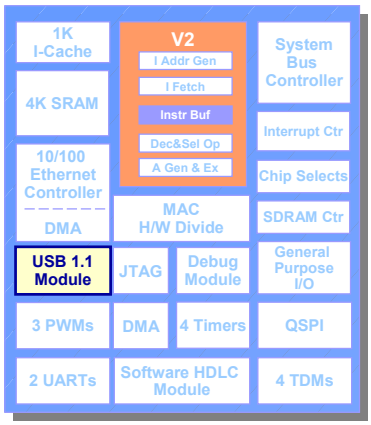
The descriptor controller opens and closes the buffer descriptors. The descriptor controller manages data flow in both transmit and receive directions. It is programmed with microcode to open and close buffer descriptors, control the transmit collision recovery process, and filter receive frame addresses. The descriptor controller accesses both the transmit and receive descriptor rings through the descriptor access block. The descriptor access block acts as a dedicated single channel DMA that either reads a descriptor in external user memory or writes an updated descriptor back into user memory.

The DMA controller manages the data transfer in the module. As soon as the DMA channel is initialized, it begins transferring data. An on-board RAM acts as both a transmit and receive FIFO, and also provides scratch memory for the FEC.

The RAM is the focal point of all data flow in the FEC. The RAM is divided into three sections: transmit FIFO, receive FIFO, and descriptor controller memory. User data flows to or from the DMA unit from the receive/transmit FIFOs. Transmit data flows from the transmit FIFO into the transmit block. Receive data flows from the receive block into the receive FIFO.

The user controls the FEC by writing into the control registers located in each block. The Control and Status Registers (CSRs) provide global control (i.e. Ethernet reset and enable) and interrupt handling. The MII block provides a serial channel for the FEC and external physical layer device to pass control and status information.

USB Device Module



- **Full compliance with the USB specification revision 1.1**
  - **Full speed USB device (12 Mbps)**
- **USB device controller**
  - **With protocol control and administration for up to 8 USB endpoints, 4 alternate settings, 16 interfaces, 16 configurations**
  - **Programmable endpoint types allow a wide variety of configurations**
  - **Separate 512-byte FIFOs for IN and OUT endpoints**
  - **Automatic processing of all required USB standard device requests**
- **On-chip or external USB transceiver**

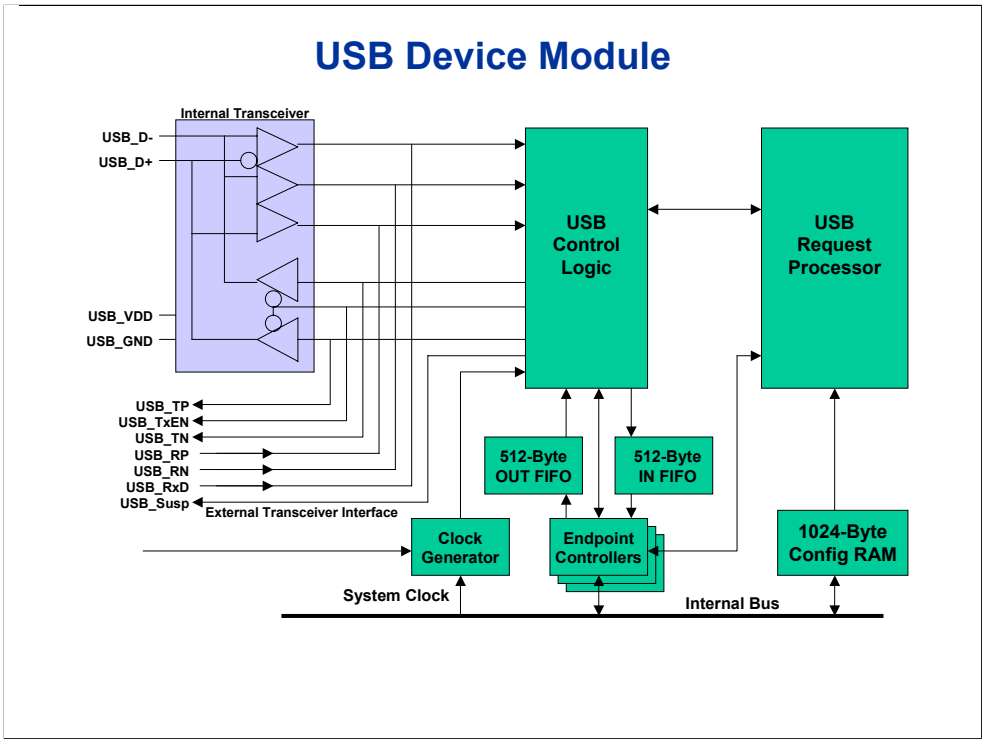
The Universal Serial Bus (USB) is an industry-standard extension to the PC architecture. The USB slave controller on ColdFire devices supports device mode data communication between itself and a USB host device, typically a PC. One host and up to 127 attached peripherals share USB bandwidth through a host-scheduled, token-based protocol.

The USB device module on ColdFire devices includes the following features; it is fully compliant with the *Universal Serial Bus Specifications, Rev 1.1,* and supports full-speed 12-Mbps USB devices and low-speed 1.5-Mbps devices.

ColdFire's USB device controller has a number of new features. It provides automatic processing of USB standard device requests, such as CLEAR_FEATURE, GET_CONFIGURATION, GET_DESCRIPTOR, GET_INTERFACE, GET_STATUS, SET_ADDRESS, SET_CONFIGURATION, SET_FEATURE, and SET_INTERFACE. It also has programmable 512-byte receive and 512-byte transmit FIFO buffers. In addition, it has protocol control and administration for up to eight endpoints, 16 interfaces, and 16 configurations.

There are programmable endpoint types with support for up to eight control, interrupt, bulk, or isochronous endpoints. It has independent interrupts for each endpoint. It supports remote wakeup. It detects start-of-frame and missed start-of-frame for isochronous endpoint synchronization. It controls notification of start-of-frame, reset, suspend, and resume events.

Finally, the ColdFire USB device module supports either an internal or external USB transceiver.



Now that you are familiar with the basic features of ColdFire's USB control module, let's look at how it works. The USB system consists of a protocol state machine, which controls the transmitter and receiver modules. The state machine implements only the USB function state diagram. This USB controller can serve as a USB function endpoint, but cannot serve as a USB host.

Here, you see a block diagram of the USB device module. The module is partitioned into five functional blocks: the USB internal transceiver, clock generator, USB control logic, USB request processor, and endpoint controllers.

The USB device module supports either an internal or external USB transceiver, USB_D+ and USB_D- drive USB cable D+ and D- lines, respectively. With additional external protection circuitry, equipment can be built that complies with *Universal Serial Bus Specification, Rev 1.1*. When the internal transceiver is selected, the driven outputs can be observed by using the parallel Port A if these pins are configured for USB.

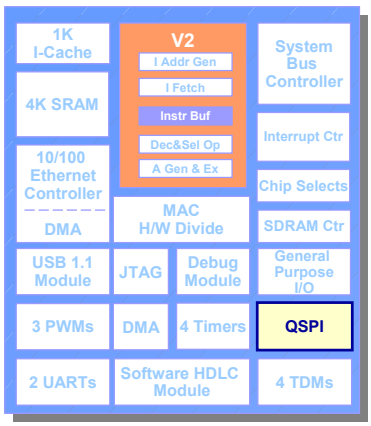
The USB device module requires two clock inputs; the system clock and a 48 MHz data clock. These are contained in the Clock Generator block.

The USB control logic performs a number of different functions. For transmitted data it performs the following: packet creation, parallel-to-serial conversion, CRC generation, NRZI encoding, and bit stuffing. For received data it performs: sync detection, packet identification, end-of-packet detection, serial-to-parallel conversion, CRC validation, NRZI decoding, and bit unstuffing. Finally, for error detection, it performs the following: bad CRC, timeout waiting for end-of-packet, and bit stuffing violations.

The USB device module has eight independent endpoint controllers that manage data transfer between the on-chip CPU and the USB host for each endpoint. These controllers provide event notification to the user and manage the IN and OUT FIFO dual-port Random Access Memory (RAM) buffers.

Finally, the ColdFire USB request processor automatically processes all of the USB standard requests listed in each ColdFire processor's specific manual (unless otherwise indicated).

QSPI Module



- **Serial interface to control external peripherals or transfer data**
- **Programmable bit rates, clock polarity and phase**
- **End-of-transmission interrupt flag, master-master mode fault flag**
- **Programmable queue : Up to 16 pre-programmed transfers**
- **Wraparound transfer mode with no CPU overhead**
- **Programmable transfer length, transfer delay, queue pointer**
- **Four programmable peripheral chip-selects**
  - **One dedicated chip select output**
  - **Three chip selects multiplexed with other pin functions**
  - **general purpose I/O port pins can be used as chip selects**

Another important component of ColdFire is the Queued Serial Peripheral Interface (QSPI) module. This module provides a serial peripheral interface with queued transfer capability. It allows users to queue up to 16 transfers at once, eliminating CPU intervention between transfers. The RAM within the QSPI is indirectly accessible using address and data registers.

Functionality is very similar, but not identical, to the QSPI portion of the Queued Serial Module (QSM) implemented in the long-time popular MC68332. It includes a serial interface to control external peripherals or transfer data. It also has programmable bit rates that clock polarity and phase. In addition, it includes an end-of-transmission interrupt flag and master-master mode fault flag.

The QSPI has a programmable queue that includes up to 16 pre-programmed transfers. It also has a wraparound transfer mode with no CPU overhead. The module has a programmable transfer length, a transfer delay, and a queue pointer.

The module has four programmable peripheral chip-selects including: one dedicated chip select output, three chip selects, multiplexed with other pin functions, and general purpose I/O port pins can be used as chip selects.

Question

Which of the following are features of ColdFire V2's USB controller module? Select all that apply.

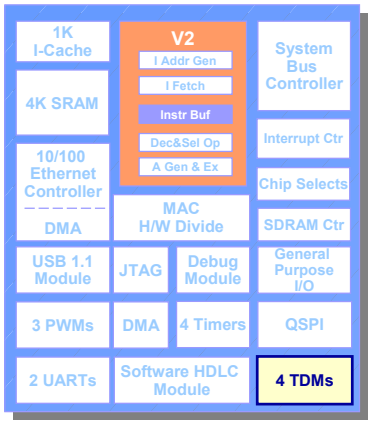
- It has programmable 512-byte receive and 512-byte transmit FIFO buffers.
- It has protocol control and administration for up to eight endpoints, 16 interfaces, and 16 configurations.
- There are programmable endpoint types with support for up to eight control, interrupt, bulk, or isochronous endpoints.
- It has independent interrupts for each endpoint.
- It has automatic internal flushing of the receive FIFO for runts and collisions.

Consider this question about the ColdFire family of products.

All the correct choices are in green

ColdFire's V2 has programmable 512-byte receive and 512-byte transmit FIFO buffers, protocol control and administration for up to eight endpoints, 16 interfaces, and 16 configurations, programmable endpoint types with support for up to eight control, interrupt, bulk, or isochronous endpoints. It also has independent interrupts for each endpoint. Automatic internal flushing of the receive FIFO for runts and collisions is a feature of the fast Ethernet MAC module, not the USB controller module.

PLIC



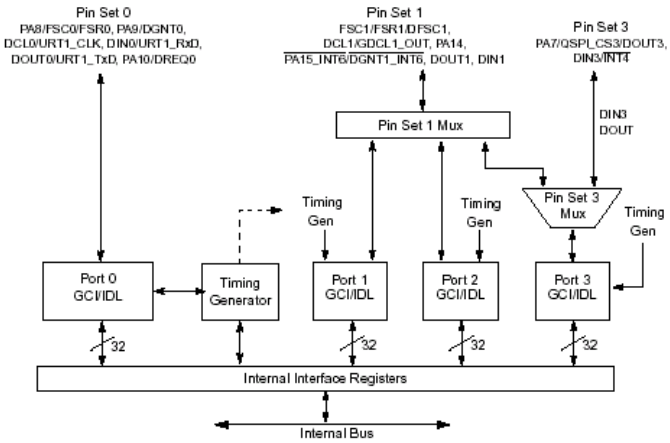
- **Primarily intended to facilitate the interface with ISDN transceivers or codecs**
- **Connects at the physical layer with devices featuring:**
  - **Interchip Digital Link (IDL)**
  - **General Circuit Interface (GCI)**
- **4 TDM ports**
-
- **Each IDL / GCI port supports 2B+D data transfer**

The Physical Layer Interface Controller (PLIC) allows the MCF5272 to connect at a physical level with external Coder/Decoders (CODECs) and other peripheral devices that use either the General Circuit Interface (GCI) or Interchip Digital Link (IDL) physical layer protocols. This module is primarily intended to facilitate designs that include Integrated Services Digital Network (ISDN) interfaces.

The MCF5272 has four dedicated physical layer interface ports for connecting to external ISDN transceivers, CODECs, and other peripherals. There are three sets of pins for these interfaces. Port 0 has its own dedicated set of pins. Ports 1, 2, and 3 share a set of pins. Port 3 can also be configured to use a dedicated pin set. Ports 1, 2, and 3 always share the same Data Clock (DCL).

When the ports are operated in slave mode, the PLIC can support a DCL frequency of 4.096 MHz and Frame Sync Frequency (FSC/FSR) of 8 KHz. When in master mode, DCL should be no greater than one-twentieth of the CPU clock (CLKIN), with a maximum FSC/FSR of 8 KHz.

PLIC



Now that you've learned the general features of the PLIC, we'll look at it in more detail. This diagram depicts the PLIC from the perspective of connecting it to an ISDN transceiver with 8-KHz frame sync. The ColdFire PLIC has four ports, Port 0 through Port 3. A port can service, read, or write any 2B + D-channel. These ports are connected through three pin sets, numbered 0, 1, and 3. Pin set 3 consists of data in and data out. Data clock and frame sync are common to pin set 1 and 3. In the case of set 1, which connects multiple ports, separate delayed frame sync generators are provided for each port which distinguish each port's active time slots.

The four ports have a number of different timing and connectivity features. Port 0 connects through pin set 0. Operates as a slave-only port; that is, an external device must source Frame Sync Clock/Frame Sync Receive (FSC/FSR) and Data Clock (DCL). These pins are unidirectional inputs. DIN0 and DOUT0 are dedicated pins for Port 0.

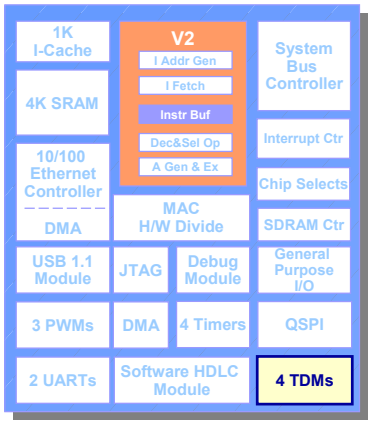
Port 1 connects through pin set 1. It operates as a master or slave port. In slave mode an external device must source FSC/FSR and DCL. In master mode, DCL1 and FSC1/FSR1 are outputs. These signals are in turn derived from the DCL0 and FSC/FSR from Port 0. For Port 1 to function in master mode, Port 0 must be enabled with an external transceiver sourcing DCL and FSC/FSR. The physical interface pins DIN1 and DOUT1 serve Ports 1, 2, and 3.

Port 2 connects through pin set 1. It operates as a slave-only port and shares a data clock with Port 1. It shares DCL1 when Port 1 is in slave mode or GDCL when Port 1 is in master mode. A delayed frame sync, DFSC2, derived from FSC1, is connected to the DFSC2 output and fed to the Port 2 IDL/GCI block. Users can synchronize the Port 2 IDL/GCI block with an offset frame sync, (offset with respect to the Port 1 GCI/IDL block), by programming the Port 2 Sync Delay Register (P2SDR).

Port 3 connects through pin set 1 or 3. It operates as a slave-only Port and shares a data clock with Port 1. It shares DCL1 when Port 1 is in slave mode, or GDCL, when Port 1 is in master mode. A delayed frame sync, DFSC3, is derived from FSC1 and is fed to the Port 3 IDL/GCI block. Programming the Port 3 sync delay register, P3SDR, allows it to be synchronized with an offset frame sync (offset with respect to the Port 1 GCI/IDL block). Port 3 can also have dedicated data in and data out pins, DIN3 and DOUT3 of pin set 3. This allows the ColdFire device to connect to ISDN NT1s that have a common frame sync and clock, but two sets of serial data-in and data-out pins.

The MCF5272 PLIC provides two sets of D-channel arbitration control pins: DREQ0 and DGNT0 for pin set 0, and DREQ1 and DGNT1 for pin set 1. Finally, because pin set 1 connects Ports 1, 2, and 3, these ports do not have D-channel arbitration control signals.

TDM Ports Configuration



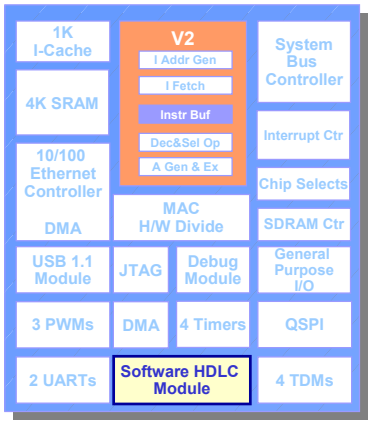
- **Port 0**
  - One Set of Pins used for Standard IDL / GCI Port with Pins for D Channel Passive Bus Arbitration
- **Ports 1, 2 & 3**
  - Pins to allow Port 1 Support for D Channel Passive Bus Arbitration
  - Ports 2 & 3 Share Common Frame Sync & Clock with Port 1
  - Delayed Frame Sync Generation for Ports 1, 2 & 3
  - Ports 1, 2, & 3 can be used for Codecs or additional transceivers
- **Port 3 can be used as dedicated port**
  - Shares common clock with Port 1
  - Delayed frame sync DFSC3 used to align frame.
  - Multiplexed with other pin functions

Here is some configuration information for the 4 TDM Ports. Port 0 has one set of pins used for standard IDL/GCI port with pins for D-channel Passive Bus Arbitration.

Ports 1, 2 & 3 have pins to allow Port 1 to support D Channel Passive Bus Arbitration. Ports 2 & 3 share common Frame Sync & Clock with Port 1. Ports 1, 2 & 3 also have delayed Frame Sync Generation and can be used for Codecs or additional transceivers.

Port 3 can be used as a dedicated port that shares common clock with Port 1. It also has delayed frame sync DFSC3 used to align the frame and is multiplexed with other pin functions.

HDLC Software Module



- **HDLC software module :**
  - Supports multiple channels simultaneously
  - Can be assigned to any B or D channel
  - Contains:
    - **CRC generation/verification, bit stuffing/unstuffing**
    - **Table lookup based framer/deframer**
    - **Shared or separate opening/closing flags**
    - **Aborted and erroneous frame counter**
  - Supports LAPB, LAPD, X.25, etc…
  - Address filtering asynchronous speed up to 250 Kbps, synchronous speed up to 500Kbps
- **Provided as linkable object module with documented API**

ColdFire HLDC Software is available at www.freescale.com

Another module in ColdFire is the High Level Data Link Control (HDLC) software module. The HDLC is a bit-oriented open systems interconnection (OSI) Layer 2 protocol commonly used in data communications systems. Many other common layer 2 protocols, such as, ISDN LAP-B, ISDN LAP-D, and Ethernet, are heavily based on HDLC.

The peripheral independent main software block is capable of running on any ColdFire Version 2 (V2) based processor. However, the software object module, as delivered, assumes the presence of a number of tables in ROM, currently only present on the MCF5272 device

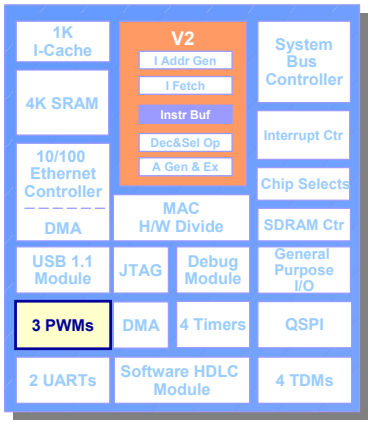
The soft HDLC function implements an HDLC framer/deframer function.

The ColdFire HDLC transmit (Tx) features include: it operates at 56 or 64 Kbps, it has the CRC calculation option, it can abort transmission at any frame boundary, and it fills the output buffer with ones or flags as needed.

The ColdFire HDLC receive (Rx) features include: it operates at 56 or 64 Kbps, it enables or disables CRC checking, it reports the number of CRC errors and aborts to calling function, it has address recognition of up to three independent addresses per channel - two regular independent addresses, one independent address associated with a mask, and the broadcast address. It also recognizes 0-, 8-, or 16-bit addresses. Finally, it restarts reception on any frame boundary.

The MCF5272 ColdFire HDLC software module is available on the website (www.freescale.com) **for free** via a “click” software license agreement. The software is delivered to the licensee in object format library (tixxx\libhdlc.a) ready to be linked together with the customer’s own software. It consists of two main functions: HDLC_Tx_Driver and HDLC_Rx_Driver.

PWM Module

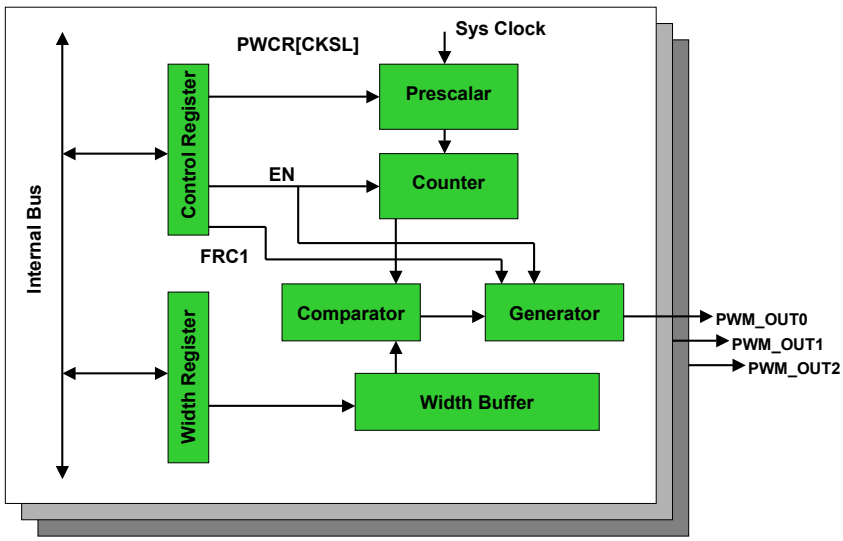


- **Used for Audio Tone Generation along with External R/C Integrator**
- **Features :**
  - **3 Output Compare Pins**
  - **Double-Buffered Width Register**
  - **Variable-Divide Prescale**
  - **Three Independent PWM Modules**
  - **Byte-wide Width Register Provides Programmable Control of Duty Cycle**

The Pulse Width Modulation (PWM) module is another component of ColdFire V2. It generates a synchronous series of pulses having a programmable duty cycle. With a suitable low-pass filter, the PWM can be used as a digital-to-analog converter. It is used for audio tone generation along with the external R/C integrator.

The PWM has the following features: three output compare pins, a double-buffered width register, variable-divide prescale, three independent PWM modules, and byte-wide width register provides programmable control of duty cycle.

PWM Module



Let's look at the PWM module in more detail. The PWM is a simple free-running counter combined with a pulse width register and a comparator such that the output is cleared whenever the counter value exceeds the width register value. When the counter overflows, or "wraps around," its value becomes less than or equal to the value of the width register, and the output is set.

The width register is double-buffered so that a new value can be loaded for the next cycle without affecting the current cycle.

At the beginning of each period, the value of the width register is loaded into the width buffer, which feeds the comparator. This value is used for comparison during the next cycle.

The prescalar contains a variable divider that can reduce the incoming clock frequency by certain values between 1 and 32768.

Question

True or false: The MCF5272 has four dedicated physical layer interface ports for connecting to external ISDN transceivers, CODECs, and other peripherals.

TRUE

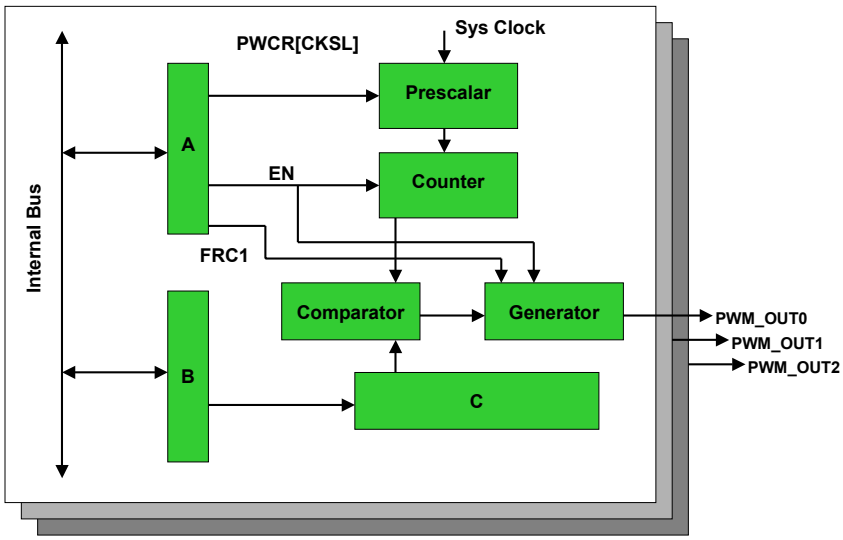
FALSE

Consider this question about the ColdFire family of products.

The correct answer is TRUE. The MCF5272 has four dedicated physical layer interface ports for connecting to external ISDN transceivers, CODECs, and other peripherals.

Question

Which block within the PWM module is the width buffer; A,B or C?
Click the correct box.



Consider this question about the PWM module.

The correct answer is C

That is the width buffer. At the beginning of each period, the value of the width buffer register is loaded into the width register, which feeds the comparator.

Module Summary

- 10/100 Fast Ethernet MAC
- USB device module
- QSPI device
- PLIC module
- PWM module

Let's review the ColdFire Application Specific Peripherals that we examined in this module. First we learned the features and operation of the 10/100 Fast Ethernet MAC. Then we learned the attributes and functionality of the universal serial bus device module. Next, we examined the features and operations of the queued serial peripheral interface module. Then we reviewed the physical layer interface module's features and operations. Finally, we learned the attributes and operations of the pulse width modulation module.